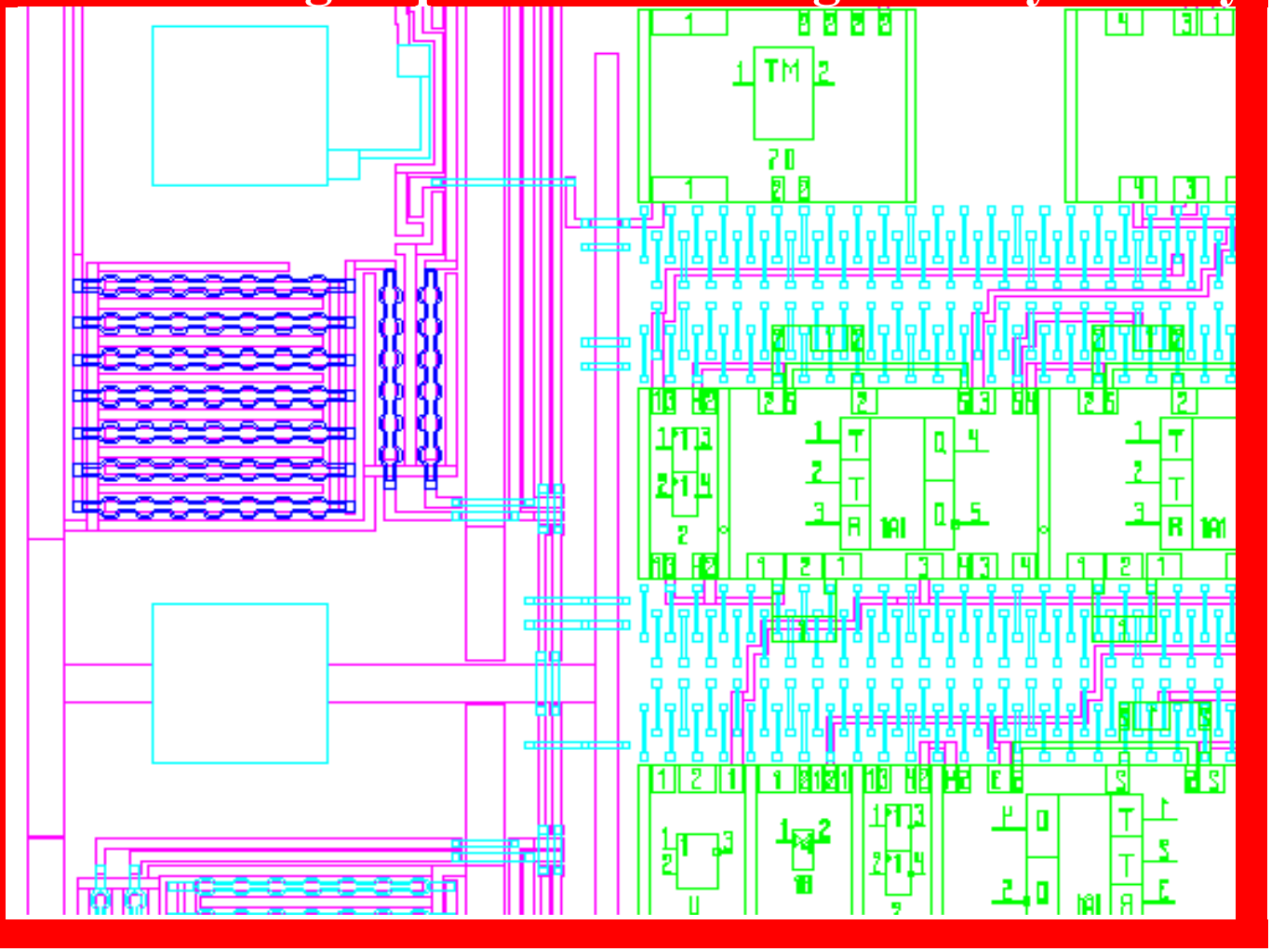
S Y N T E C

HCMOS
LOGIC ARRAYS

The 1580 High Speed CMOS Logic Array Family



The 1580 High Speed CMOS Logic Array Family

The Syntec 1580 Family of high speed CMOS logic arrays is specifically designed to allow the user to easily integrate custom LSI logic into his total system design.

The technology used for the 1580 family is Syntec's mainstream two micron silicon gate CMOS process which result in 2.0 nanosecond gate delays whilst driving ten internal loads and still maintaining the low power consumption associated with CMOS .

A wide range of interface options are available enabling the arrays to interface directly with both low power schottky and CMOS systems .

The complete 1580 family is fully compatible with 54/74HC high speed CMOS logic building blocks .

The 1580 family also offers a high drive capability of 50 mA (for both sink and source) coupled with electrostatic discharge protection of plus/minus 2 kV . Positioning of guardrings around all input and output geometries protect the arrays from the traditional CMOS problem of latchup .

All Members of 1580 family are designed to make use of plastic DIL , SOIC and ceramic DIL or plain packaging .

FEATURES

DRIVE
50 mA . Sink and source capability

FEATURES

SPEED
2.0 nanosecond . Delay at 10 loads

FEATURES

RELIABILITY
500 mA latchup immunity
±2 kV ESD protection

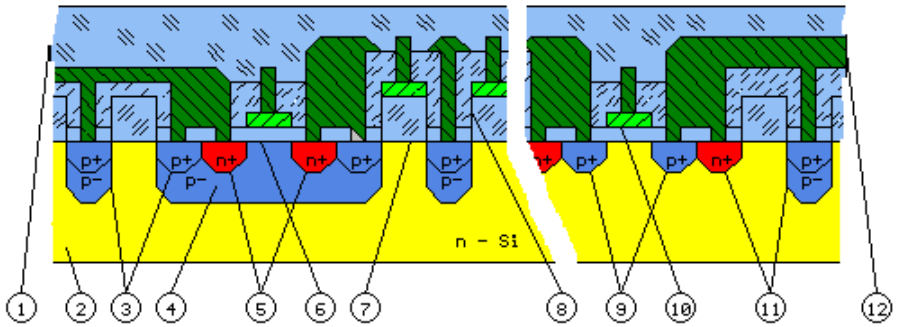
1580	Gate equiva lent *	I/O	PACKAGE OPTIONS		
			8	14	16
XM3	200	14			
XM5	300	14			

* - 2 input NAND/NOR

FEATURES

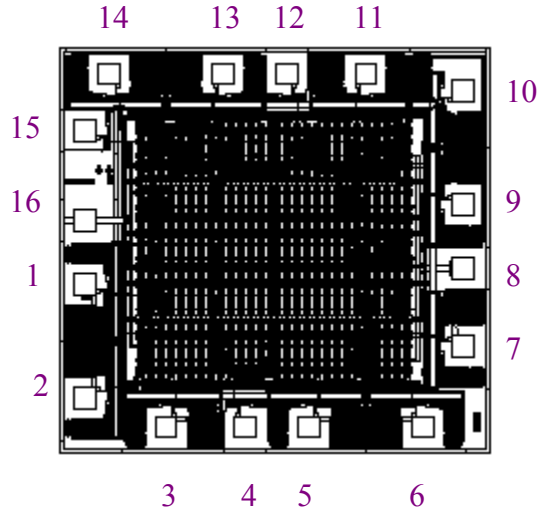
FLEXIBILITY
CMOS and TTL compatible I/O on all pins

1. Protection oxide .
2. Substrate (N) .
3. Guardrings (P) .
4. P-well .
5. Source / Drain N-Channel Transistor .
6. Thin gate oxide .
7. Thick field oxide .
8. Isolation oxide .
9. Source / Drain P-Channel Transistor .
10. Polysilicon Gate .
11. Guardrings (N) .
12. Metal (Al) layout .



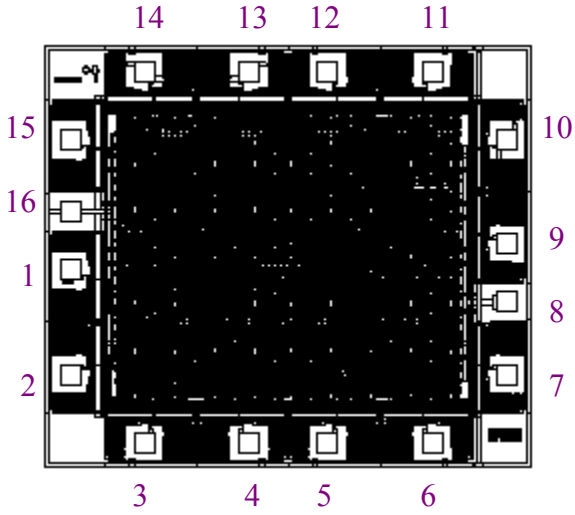
Dimensions and Connection Diagram

КР1580ХМ3



Dimensions: X – 2.69 mm, Y – 2.54 mm.

КР1580ХМ5



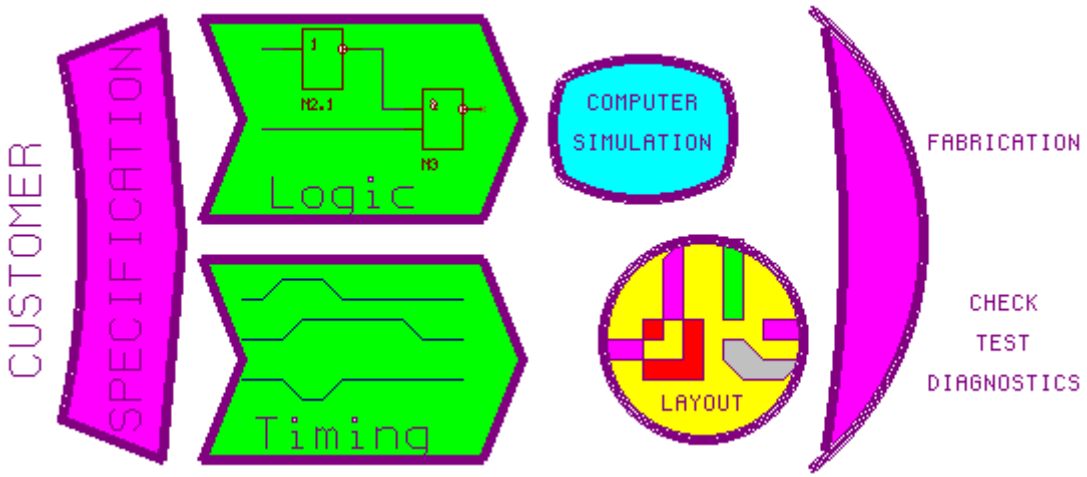
Dimensions: X – 3.26 mm, Y – 2.85 mm.

Pin description.

Pad number	КР1580ХМ3	КР1580ХМ5
1.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
2.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
3.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
4.	Input	Universal pin (pad) – input-output
5.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
6.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
7.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
8.	Ground	Ground
9.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
10.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
11.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
12.	Input	Universal pin (pad) – input-output
13.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
14.	Universal pin (pad) – input-output	Universal pin (pad) – input-output
15.	Input	Universal pin (pad) – input-output
16.	Supply voltage	Supply voltage

Gate arrays are build by principle of "Gates Sea". A basic structure unit is inverter gate. KP1580XM3 chip consist of 400 gates and KP1580XM5 – 600 ones .	Logic elements library include up to 90 elements varieties of the next basic classes - - logic elements (NOT , NOR , NAND with various numbers of inputs) ; - triggers (D- triggers, RS- triggers, Schmitt-triggers, etc.) ; - buffers and drivers (with various load characteristics) ; - analog and digital multiplexers; - TTL to CMOS converters.

The Design Automation System



DC and AC characteristics over temperature range

Parameter , units	Symbol	Rate		Conditions				Temperature , °C
		min	max	Ucc, B	Uil, B	Uih, B	Io, мА	
1. Output LOW voltage, V	Uol		0.10	3.0	0.6	2.10	0.02	-10, +25, +85
				4.5	0.9	3.15		
				6.0	1.2	4.20		
			0.26	4.5	0.9	3.15	4.0	+25
			0.40					-10 , +85
2. Output HIGH voltage, V	Uoh	2.90		3.0	0.6	2.10	0.02	-10, +25, +85
		4.40		4.5	0.9	3.15		
		5.90		6.0	1.2	4.20		
		3.98		4.5	0.9	3.15	4.0	+25
		3.60						-10 , +85
3. Input leakage current, µA	Iil Iih		0.1	6.0	0.0	6.0	-	+25
			1.0					-10 , +85
4. 3-state output leakage current, µA	Iozl Iozh		0.5	6.0	0.0	6.0	-	+25
			5.0					-10 , +85
5. Quiescent device current, µA	Icc		1.0	6.0	0.0	6.0	-	+25
			10.0					-10 , +85
5. Propagation delay, ns/inverter	tplh , tphl		5.0	4.5	0.0	4.5	-	+25
			10.0					-10 , +85

Recommended operating conditions and absolute maximum ratings.

Parameter , units	Symbol	Ratings and conditions			
		recommended		absolute maximum ratings	
		min	max	min	max
1. DC supply voltage, V	Ucc	3.0	6.0	-0.5	9.0
2.Input LOW voltage, V	Uil		0.2 Ucc	-0.5	
3. Input HIGH voltage, V	Uih	0.7 Ucc			**Ucc+0.5**
4. DC output current, mA	Io		30		50
5. DC device current, mA	Icc		50		100
6. Input rise/fall time, ns	tr				500
7. Power dissipation, mW	P				300
8. Max load capacity, pF	Cmax				500
9. Operating/storage temperature, °C	T	-10	+85	-60	+100

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